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EUROPEAN PATENT APPLICATION

(54) Image processing apparatus and method of controlling the same.

(57) Texture mapping is performed on polygons at the same speed as a polygon drafting process without a texture cache, thereby preventing complexity and an increase in cost. An image memory (8) is constituted in a double-buffer structure, and an address line, a data line and a memory control line are individually connected to each buffer. One of the two buffers is used for texture data, and the other for a drawing result. The texture data is one-dimensional, and the size thereof is less than a maximum value of a column address. The other buffer is an imaginary double buffer with two buffers, one of the buffers being used for reading out image data from a SAM port, the other being used for writing image data produced from polygons. Read/write switching is effected in a vertical flyback period. In the read-out buffer, just after row-directional read-out, the associated row is cleared by the flash write function of a multiport DRAM in a horizontal flyback period, and the next read-out address is output. In synchronism with this, texture data is refreshed.
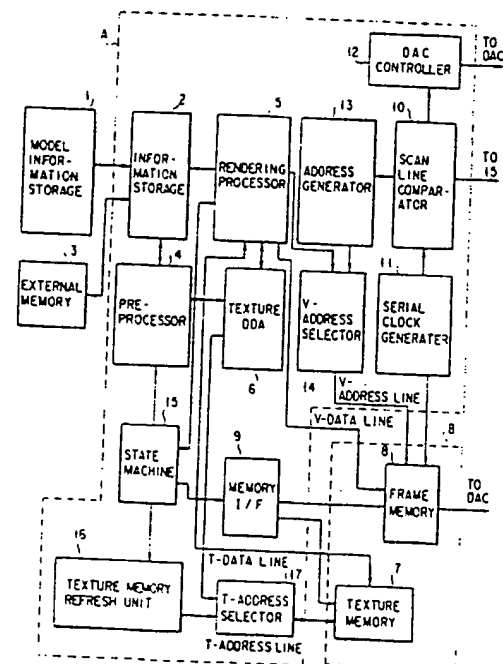

F I G. 2

EP 0 613 098 A2

The present invention relates to an image processing apparatus for performing three-dimensional (3-D) computer graphics (CG).

Recently, game machines using computer graphics (CG) have widely been prevalent. Most of them are two-dimensional (2-D) CG systems. However, images produced by CG systems are generally short of naturalness. In order to overcome this drawback, a natural image is prepared as texture data, and a model image is subjected to a texture mapping process.

A conventional inexpensive CG system has a structure as shown in FIG. 1. Specifically, a graphics chip 100 is connected to a single address line 101 and a data line 102. The address line 101 and data line 102 are connected to first and second image memories 103 and 104. Each of the image memories 103 and 104 comprises a texture data area and a pixel data area. A model produced by pixel data is painted out by texture data by the following process. At first, the graphics chip 100 fetches polygon data from an external bus 105 and then texture data from the image memory 103. The graphics chip 100 executes graphics processing and writes the processing result (pixel data) in the image memory 103. Alternatively, texture data in the image memory 104 may be fetched to subject the pixel data in the image memory 103 to mapping processing.

In the above-described conventional CG system, the graphics chip 100 does not perform in parallel the fetching of texture data and pixel data and writing in the image memory, but performs serially, and a long processing time is required. This problem results from common use of the address line and data line in two banks (image memories 103 and 104).

The reason why the address line and data line are shared by the image memories 103 and 104 is that the number of pins can be decreased and the manufacturing cost decreased. Besides, since the conventional graphics chip 100 does not include a CRT controller, it is necessary to read out data from the image memory 103 or 104 and output the data to the external bus 105. When the internal memory of the graphics chips 100 is used to output data to the external bus 105, system control is made easier by sharing the address line and data line for the image memories 103 and 104. In the conventional system, in order to simplify the mapping algorithm, texture data is stored in a two-dimensional fashion. As a result, when multiport DRAMs used as image memories 103 and 104 are accessed, a considerable page break may occur frequently. Thus, the speed of the processing for subjecting polygons to texture mapping is much lower than that of the processing for drawing only polygons. Moreover, although the multiport DRAMs

are used as image memories 103 and 104 in the conventional system, a refresh time period for refreshing a desired row address is set independently. Thus, the access to the DRAM is prohibited in the refresh time period, and the entire processing speed decreases further.

In order to solve the above problems, there is a method of providing a texture cache memory within a system or within a graphics chip and making use of it as a data buffer. However, in a video game machine whose system is inexpensive, an increase in cost due to provision of a cache memory is a problem. Furthermore, even if a cache memory is provided, since original data is two-dimensional, a considerable degree of page break occurs when texture data is fetched in the cache memory. Consequently, the processing speed lowers.

As has been described above, in the conventional 3-D computer graphics, when texture mapping is performed on polygons, the processing speed lowers and high-speed plotting cannot be achieved. Furthermore, the manufacturing cost increases due to provision of a texture cache memory.

The object of the present invention is to provide an image processing apparatus, used in a video game apparatus, for performing texture mapping on polygons at the same speed as the processing for mapping only polygons, without using a texture cache memory.

In order to achieve this object, there is provided an image processing apparatus having coordinate conversion means for conversion to a display coordinates system on the basis of model information consisting of polygons, arithmetic operation means for calculating a luminance gradient of each vertex of the polygons, means for storing the result of arithmetic operations of the arithmetic operation means, rendering means for performing shading, texture mapping, etc. of the polygons on the basis of the result of the arithmetic operations, means for storing a result of drawing in an image memory constituted basically by a multiport DRAM, and means for controlling the image memory, said apparatus comprising:

an image memory constituted by a multiport DRAM including a first memory and a second memory to which address lines, data lines, and memory control lines are individually connected;

determination means for determining whether the size of the second memory is greater than double the display size of an image to be displayed;

setting means for fixedly setting said first memory as a texture memory for storing texture data and setting said second memory as a frame memory for storing the result of drawing, if the size of the second memory is greater than double the

display size, said setting means also setting the internal structure of the second memory as imaginary double buffers divided by information of a highest bit for the address data, the internal data structure of said texture memory being such that two-dimensional texture data is expressed as one-dimensional texture data, the side of the one-dimensional texture data being less than a maximum value of a column address of said first memory;

buffer switching means for switching, within a vertical flyback time period, double buffers set within the second memory such that one of said buffers is used for reading out image data from a SAM (serial access memory) port, and the other of said buffers is used for writing image data produced from the polygons into a RAM port;

detecting means for detecting completion of reading out of the image data of every scan line of said buffer for reading out the image data;

clearing means for clearing the scan line detected by said detecting means within a horizontal flyback time period (horizontal blanking time period) by means of a flash write function of said multiport DRAM;

next-address output means for outputting an address of the next-readout scan line of the scan line cleared by said clearing means; and

refreshing means for refreshing the texture memory in synchronism with the clearing processing of said clearing means and the address output from said next-address output means.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1. is a view for explaining a method of using a conventional image memory;

FIG. 2 shows the structure of an embodiment of the present invention;

FIG. 3 shows an example of the contents of a texture memory used in the apparatus shown in FIG. 2; and

FIG. 4 is a timing chart for explaining the operation of the apparatus shown in FIG. 2.

An embodiment of the present invention will now be described with reference to the accompanying drawings.

FIG. 2 shows the structure of an image processing system apparatus according to an embodiment of the present invention.

In FIG. 2, a block indicated by a broken line A is a graphics chip, and a block indicated by a broken line B is an image memory. The image memory B comprises a well-known multiport DRAM.

In this system, the image memory B has a double-buffer structure (a texture memory 7 and a frame memory 8 are shown in FIG. 2). Each buffer (texture memory 7, frame memory 8) is individually connected to an address line, a data line and a memory control line.

The frame memory 8 is used for storing the result of drawing, and the texture memory 7 is used for storing texture data.

The internal data array of the texture memory 7 is a one-dimensional texture data array and the size of the one-dimensional texture data is less than the maximum value of column addresses of the memory. The internal structure of the frame memory 8 is divided by information of a highest bit for the address data, and one frame memory 8 is used as an imaginary double buffer memory. One buffer and the other buffer are alternately switched for write and read in a vertical fly-back time period. An SAM (serial access memory) port is used as an image data read-out port, and a RAM (random access memory) port is used as an image data write port for writing of data produced by use of polygons.

When a mapping data producing process is started, the image memory B is set in the texture memory 7 and frame memory 8. Then, it is determined whether or not the size of the frame memory 8 is greater than double the display size of image. This determination is effected when the system is powered on. Predetermined data is written from the top address in the image memory B via a V data line. And the data is read out from the image memory B. The read-out data is monitored by a system controller (not shown), and thereby the size of the image memory B is determined. If the size of the frame memory 8 is greater than double the display size of image, the frame memory 8 is used as imaginary double buffers. The screen display size is determined, e.g., in accordance with the size of a model to be mapped.

The structure and operation of the entire system will now be described.

Polygon-based model information (coordinate values of display of each vertex, luminance, texture coordinate values, etc.) is stored a model information storage 1 such as a ROM cassette, hard disk, or CD-ROM. Polygons are information including basic cell data for 3-D mapping.

Polygon information constituting a model is stored directly in an information storage 2, or it is temporarily stored in an external memory 3 and then stored in the information storage. A pre-processor 4 subjects a model stored in the information storage 2 to, e.g. transformation (affine transformation) from world coordinates to viewpoint coordinates or perspective transformation. The information obtained by this transformation process is transferred to the information storage or external memory 3. After the pre-processor 4 has completed pre-processes, such as coordinate trans-

formation, perspective transformation, planar formula processing, luminance gradient processing, with respect to all polygons. each polygon information item is transferred from the information storage 2 or external memory 3 to a drafting processor 5. The rendering processor 5 performs analysis processing by DDA (Digital Differential Analysis) such as shading of polygons. When texture is mapped on polygons subjected to a rendering arithmetic operation. i.e. shading processing, a texture number of a texture to be mapped on model (polygon) information and texture coordinates corresponding to vertices of polygons are read out of the information storage 2 and transferred to a texture DDA 6. The DDA6 calculates an address in the texture memory 7 corresponding to each pixel of polygons on the basis of texture coordinates of vertices of polygons.

In FIG. 2, the texture memory and frame memory 8 are shown as separate units. However, as described above. they are constituted by the multiport DRAM. In this system, the image memory (multiport DRAM having a flash write function) has a double buffer structure. and address lines, data lines and memory control lines are separately connected to the individual buffers. One of the buffers is used as texture memory 7 for storing texture data, and the other as frame memory 8 for storing the result of drawing.

The address calculated by the texture DDA 6 is selected by a T-address selector 17 and transferred to the texture memory 7 via a T-address line. Then. the texture data is transferred from the texture memory 7 to the rendering processor 5 via a T-data line. The rendering processor 5 executes processes such as α -Blending. thereby producing drawing data. The drawing data is supplied to the frame memory 8 via a V-data line.

On the other hand. a V-address selector 14 obtains from a state machine 15 information to the effect that the present mode is the drawing mode, and selects an address from the rendering processor 5. The selected address is led to the V-address. Thereby. the drawing data is stored in the frame memory 8.

In these processes. the calculation of the texture coordinates by the texture DDA6 is effected in units of a pixel and therefore it is effected in synchronism with the DDA processing for shading carried out in the rendering processor 5. thus enabling pipeline processing to be performed.

FIG. 3 shows the structure of texture data within the texture memory 7. Specifically, two-dimensional texture data is stored in the state in which it is expressed as one-dimensional texture data.

When texture data is constituted within the texture memory 7 in the above manner. all texture data relating to one texture is present one-dimensionally within a page in the DRAM. Thus. only by controlling a memory control signal (row address strobe (RAS),etc.) necessary for first accessing to a page in the memory 7. can the high-speed page mode operation or pipeline mode operation peculiar to the DRAM be performed. While a single texture mapping operation is performed. no page break occurs. and a high-speed drawing process can be executed without break of pipe. The memories 7 and 8 are controlled by control signals from a memory interface (memory I:F)9. Data is read out from the aforementioned other buffer of the frame memory 8. and the read-out data is fed to a DAC (digital-to-analog converter). At this time. a scan line comparator 10 counts a scan-line-directional image read-out serial clock produced by a serial clock generator 11. and determines whether or not data transfer corresponding to the number of pixels in the scan line direction has been completed. If it is completed. end signals are fed to the state machine 15 and a DAC (digital-to-analog converter) controller 12. Then. the state machine 15 sends processing pause information to the rendering processor 5. On the other hand. the DAC controller 12 outputs a horizontal blanking signal.

An end signal is also sent to an address generator 13. Then. the address generator 13 outputs a row address of a scan line from which data read-out has been finished and supplies the row address to a V-address selector 14. In addition. the state machine 15 sends flyback mode information to the V-address selector 14. Thereby. the V-address selector 14 selects the row address from the address generator 13 and outputs it to a V-address line. In this case. a flash write operation of the multiport DRAM is used. and the control signal is output from the memory I:F 9. The stored data relating to the associated line is cleared by the flash write. Thereafter. for reading out the next image data, a row address is generated by the address generator 13 and output to the V-address line. Thereby. in the read-out side buffer of the frame memory 8. data is transferred to the SAM port and the data can be read out.

As described above. a flyback mode is set in part of the horizontal flyback time period. and information from the address generator 13 flows in the V-address line. Thus. the drafting processing in the drafting processor 5 is not effected.

By making use of this time period (part of the horizontal low address strobe). the texture memory 7 is refreshed in the RAS (low address strobe)-only-refresh type mode. Specifically. when a texture memory refresh unit 16 receives flyback mode information from the state machine 15. it produces a row address (n) to be refreshed. The T-address selector 17 selects the row address (n) from the texture memory refresh unit 16 and outputs it to

the texture memory 7 for RAS-only-refresh. Subsequently, the texture memory refresh unit 16 produces a row address (n + 1) and refreshes the (n + 1)th address similarly. After refreshing, the operation mode of the T-address selector 17 is changed to the drafting mode by a command from the state machine 15, and it selects a T-address line from the texture DDA 6.

The reason why the two row addresses of the texture memory 8 can be refreshed in synchronism with the control of the frame memory 8 is as follows: since the timing for clearing the stored content of the row address immediately after read-out and the timing for designating the next read-out row address are provided for the frame memory 8, the address is supplied twice and the texture memory 7 and frame memory 8 are constituted in the DRAM.

After the image data has been read out from one of the buffers of the frame memory 8, the data relating to the vertical flyback time period is sent to the state machine 15, and the said one of the buffers is used for data write and the other for data read. The switching between the read mode and write mode of both buffers is effected by data fed from the state machine 15 via the I/F 9.

FIG. 4 shows a simple timing chart of the present system.

An upper portion of FIG. 4 illustrates a timing of the frame memory 8, showing a row address m of a scan line and a row address (m + 1) for the next read-out. At the time the row address (m + 1) is designated, the stored data is transferred to the SAM port side within the memory 8. A lower portion of FIG. 4 illustrates a timing of the texture memory 7. In synchronism with the address control of the frame memory 8, the address m and address (m + 1) of the texture memory 7 are refreshed. In this manner, by refreshing the addresses of two rows of the texture memory 7, the texture memory 7 can be refreshed at a speed twice as high as the read-out speed of the frame memory 8.

As has been described above, according to this invention, there is provided an image processing apparatus having coordinate conversion means for conversion to a display coordinates system on the basis of model information consisting of polygons, arithmetic operation means for calculating a luminance gradient of each vertex of the polygons, means for storing the result of arithmetic operations of the arithmetic operation means, rendering means for performing shading, texture mapping, etc. of the polygons on the basis of the result of the arithmetic operations, means for storing a result of drawing in an image memory constituted basically by a multiport DRAM, and means for controlling the image memory. In this apparatus, an image memory (B) constituted by a multiport DRAM includes a first

memory (7) and a second memory (8) to which address lines, data lines, and memory control lines are individually connected. Determination means (20) determines whether the size of the second memory (8) is greater than double the display size of an image to be displayed. Setting means (15, 9) sets fixedly the first memory (7) as a texture memory for storing texture data and sets said second memory (8) as a frame memory for storing the result of drawing, if the size of the second memory (8) is greater than double the display size. The setting means also sets the internal structure of the second memory (8) as imaginary double buffers divided by information of a highest bit for the address data. Of the imaginary double buffers, one of said buffers is used for reading out image data from a SAM (serial access memory) port, and the other of said buffers is used for writing image data produced from the polygons into a RAM port. In the internal data structure of the texture memory, two-dimensional texture data is expressed as one-dimensional texture data, the size of the one-dimensional texture data being less than a maximum value of a column address of said first memory. Buffer switching means (9, 15) switches, within a vertical flyback time period, the double buffers set within the second memory (8) so that one of them is used for data read and the other for data write. Detecting means (10, 11) detects completion of reading out of the image data of every scan line of said buffer for reading out the image data. Clearing means (13, 14, 15, 9) clears the scan line detected by said detecting means within a horizontal flyback time period (horizontal blanking time period) by means of a flash write function of said multiport DRAM. Next-address output means (13, 14, 15, 9) outputs an address of the next-readout scan line of the scan line cleared by said clearing means. Refreshing means (15, 16) refreshes the texture memory in synchronism with the clearing processing of said clearing means and the address output from said next-address output means.

By the above means, in the image processing apparatus for performing 3-D computer graphics, the image memory (B) using the multiport DRAM is set as texture memory 7 and frame memory 8. If the size of the memory 8 is greater than twice the screen size, one of the memories is used for storing drafting data, and the other for storing texture data. Flash write is effected on the line which has completely been read in the horizontal flyback period. At the same time, an address for transferring data to the SAM port for read-out is generated, and synchronously the texture memory is refreshed, thereby preventing a decrease in processing speed due to the refresh cycle. In the texture memory 7, conventional two-dimensional texture data is rearranged in a one-dimensional fashion, and the tex-

ture size data is made to fall within DRAM page size. Thereby, page break does not occur and high-speed texture mapping is performed. Besides, a decrease in processing speed, which has conventionally occurred in effecting texture mapping on polygons, does not occur. The manufacturing cost does not increase owing to addition of texture caching. Therefore, inexpensive, high-speed texture mapping can be realized.

The present invention is not limited to the above embodiments, and various modifications can be made.

As has been described above, according to this invention, page break in DRAM or a decrease in processing speed due to refresh timing does not occur, and a high-speed texture mapping process can be performed without adding a texture cache memory.

Claims

1. An image processing apparatus having coordinate conversion means for conversion to a display coordinates system on the basis of model information consisting of polygons, arithmetic operation means for calculating a luminance gradient of each vertex of the polygons, means for storing the result of arithmetic operations of the arithmetic operation means, rendering means for performing shading, texture mapping, etc. of the polygons on the basis of the result of the arithmetic operations, means for storing a result of drawing in an image memory constituted basically by a multiport DRAM, and means for controlling the image memory, said apparatus characterized by comprising:

an image memory (B) constituted by a multiport DRAM including a first memory (7) and a second memory (8) to which address lines, data lines, and memory control lines are individually connected;

determination means (20) for determining whether the size of the second memory (8) is greater than double the display size of an image to be displayed;

setting means (15, 9) for fixedly setting said first memory (7) as a texture memory for storing texture data and setting said second memory (8) as a frame memory for storing the result of drafting, if the size of the second memory (8) is greater than double the display size, said setting means also setting the internal structure of the second memory (8) as imaginary double buffers divided by information of a highest bit for the address data, the internal data structure of said texture memory being such that two-dimensional texture data is

expressed as one-dimensional texture data, the size of the one-dimensional texture data being less than a maximum value of a column address of said first memory;

buffer switching means (9, 15) for switching, within a vertical flyback time period, double buffers set within the second memory (8) such that one of said buffers is used for reading out image data from a SAM (serial access memory) port, and the other of said buffers is used for writing image data produced from the polygons into a RAM port;

detecting means (10, 11) for detecting completion of reading out of the image data of every scan line of said buffer for reading out the image data;

clearing means (13, 14, 15, 9) for clearing the scan line detected by said detecting means within a horizontal flyback time period (horizontal blanking time period) by means of a flash write function of said multiport DRAM;

next-address output means (13, 14, 15, 9) for outputting an address of the next-readout scan line of the scan line cleared by said clearing means; and

refreshing means (15, 16) for refreshing the texture memory in synchronism with the clearing processing of said clearing means and the address output from said next-address output means.

2. The apparatus according to claim 1, characterized in that said refreshing means for refreshing said texture memory refreshes a plurality of lines in said horizontal flyback time period by a RAS-only-refresh function.

3. A method for controlling an image processing apparatus having coordinate conversion means for conversion to a display coordinates system on the basis of model information consisting of polygons, arithmetic operation means for calculating a luminance gradient of each vertex of the polygons, means for storing the result of arithmetic operations of the arithmetic operation means, rendering means for performing shading, texture mapping, etc. of the polygons on the basis of the result of the arithmetic operations, means for storing a result of drawing in an image memory constituted basically by a multiport DRAM, and means for controlling the image memory, characterized in that an image memory (B) constituted by a multiport DRAM including a first memory (7) and a second memory (8) to which address lines, data lines, and memory control lines are individually connected said method characterized by comprising:

a first step of determining whether the size of the second memory (8) is greater than double the display size of an image to be displayed;

a second step of fixedly setting said first memory (7) as a texture memory for storing texture data and setting said second memory (8) as a frame memory for storing the result of drawing, if the size of the second memory (8) is greater than double the display size, said setting means also setting the internal structure of the second memory (8) as imaginary double buffers divided by information of a highest bit for the address data, the internal data structure of said texture memory being such that two-dimensional texture data is expressed as one-dimensional texture data, the size of the one-dimensional texture data being less than a maximum value of a column address of said first memory;

a third step of switching, within a vertical flyback time period, double buffers set within the second memory (8) such that one of said buffers is used for reading out image data from a SAM (serial access memory) port, and the other of said buffers is used for writing image data produced from the polygons into a RAM port;

a fourth step of detecting completion of reading out of the image data of every scan line of said buffer for reading out the image data;

a fifth step of clearing the scan line detected by said detecting means within a horizontal flyback time period (horizontal blanking time period) by means of a flash write function of said multiport DRAM;

a sixth step of outputting an address of the next-readout scan line of the scan line cleared by said clearing means; and

a seventh step of refreshing the texture memory in synchronism with the clearing processing of said clearing means and the address output from said next-address output means.

4. An image processing apparatus characterized by comprising:

an image memory (8) constituted by a multiport DRAM including a first memory (7) and a second memory (8) to which address lines, data lines, and memory control lines are individually connected;

memory control means (9, 15) for controlling said second memory (8) so that said second memory (8) functions as imaginary double buffers divided by information of a highest bit for the address data, and switching, within a

vertical flyback time period, such that one of said buffers is used for reading out image data from a SAM (serial access memory) port and the other of said buffers is used for writing image data produced from the polygons into a RAM port;

data write means (5) for writing two-dimensional texture data in said first memory (7), with said two-dimensional texture data being expressed as one-dimensional texture data, and with the size of the one-dimensional texture data being less than a maximum value of a column address of said first memory, and writing image data in said second memory (8);

detecting means (10, 11) for detecting completion of reading out of the image data of every scan line of said buffer for reading out the image data;

clearing means (13, 14, 15, 9) for clearing, when a detection output is obtained from the detecting means (10, 11), the associated scan line within a horizontal flyback time period (horizontal blanking time period) by means of a flash write function of said multiport DRAM;

next-address output means (13, 14, 15, 9) for outputting an address of the next-readout scan line of the scan line cleared by said clearing means; and

refreshing means (15, 16) for refreshing the texture memory in synchronism with the clearing processing of said clearing means and the address output from said next-address output means.

5. The apparatus according to claim 4, characterized in that said detecting means (10, 11) includes:

a serial clock generator (11); and

a scan line comparator (10) for counting an output clock from said serial clock generator (11) and comparing the counted result with the number of pixels of one line, thereby obtaining said detection output (coincidence output).

6. The apparatus according to claim 5, characterized in that said detection output is also supplied to a controller (12) of a digital-to-analog converter for converting output data from said frame memory 8 to analog data.
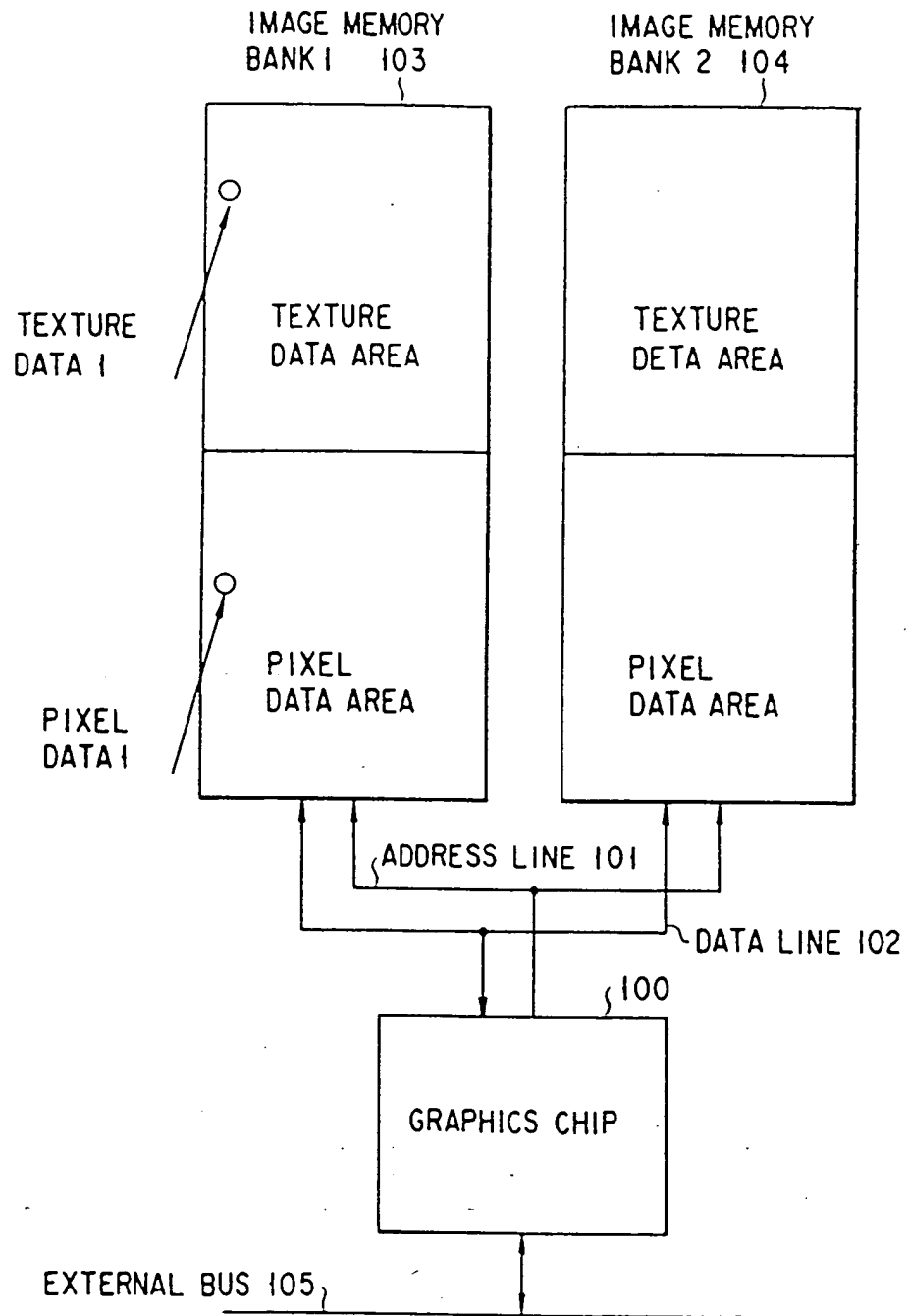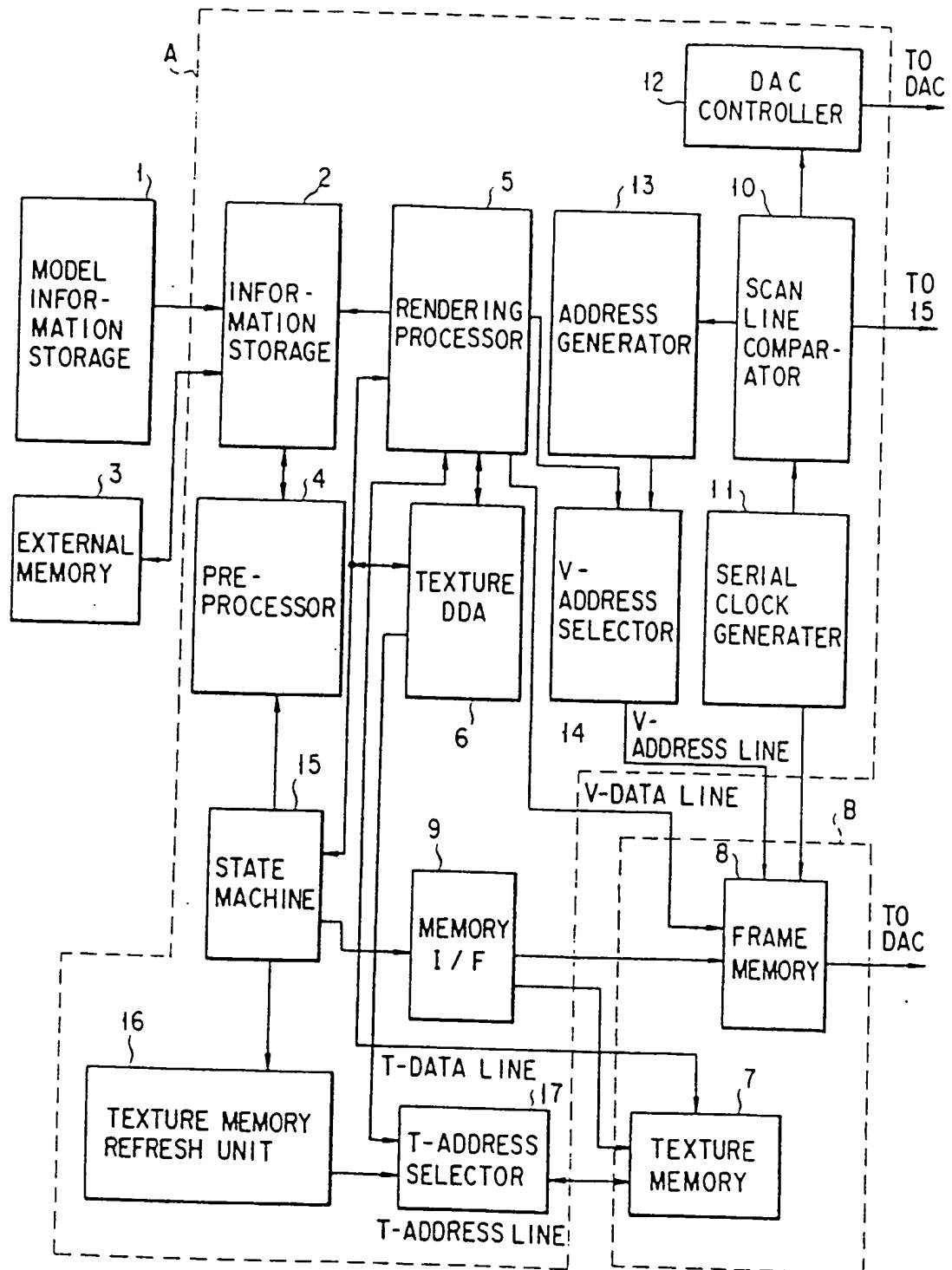
IMAGE MEMORY
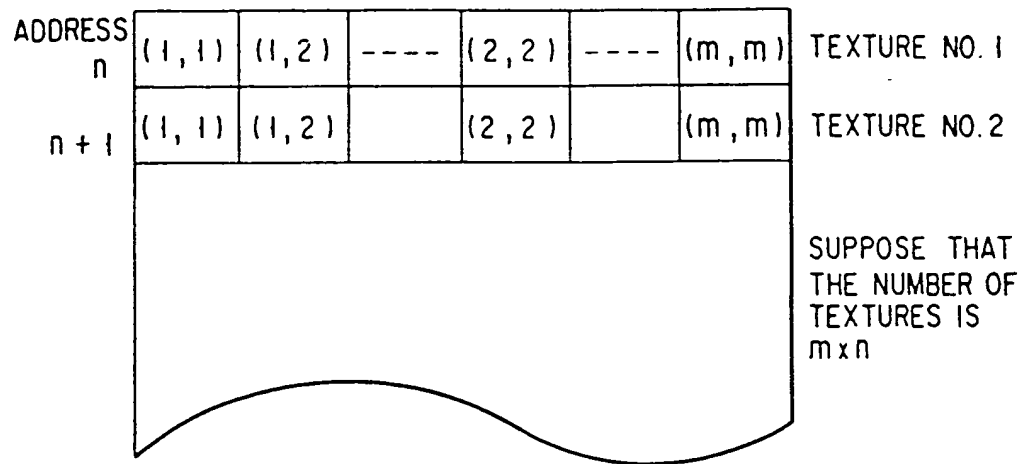BANK 1   103
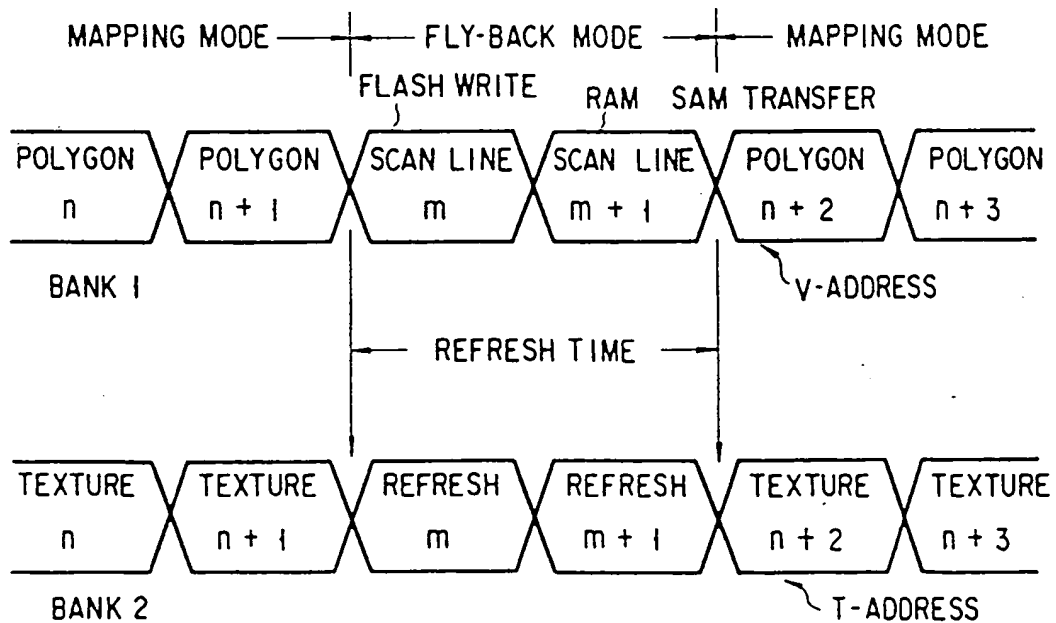
IMAGE MEMORY
BANK 2   104

TEXTURE
DATA 1

TEXTURE
DATA AREA

TEXTURE
DETA AREA

PIXEL
DATA 1

PIXEL
DATA AREA

PIXEL
DATA AREA

ADDRESS LINE 101

DATA LINE 102

100

GRAPHICS CHIP

EXTERNAL BUS 105

F I G.   1

F I G.   2

ADDRESS	(1,1)	(1,2)	----	(2,2)	----	(m,m)	TEXTURE NO. 1
n							
n + 1	(1,1)	(1,2)		(2,2)		(m,m)	TEXTURE NO. 2

SUPPOSE THAT
THE NUMBER OF
TEXTURES IS
m x n

F I G. 3

MAPPING MODE ——|—— FLY-BACK MODE ——|—— MAPPING MODE

FLASH WRITE   RAM   SAM TRANSFER

| POLYGON n | POLYGON n + 1 | SCAN LINE m | SCAN LINE m + 1 | POLYGON n + 2 | POLYGON n + 3 |

BANK I   V-ADDRESS

|←—— REFRESH TIME ——→|

| TEXTURE n | TEXTURE n + 1 | REFRESH m | REFRESH m + 1 | TEXTURE n + 2 | TEXTURE n + 3 |

BANK 2   T-ADDRESS

F I G. 4

EUROPEAN PATENT APPLICATION

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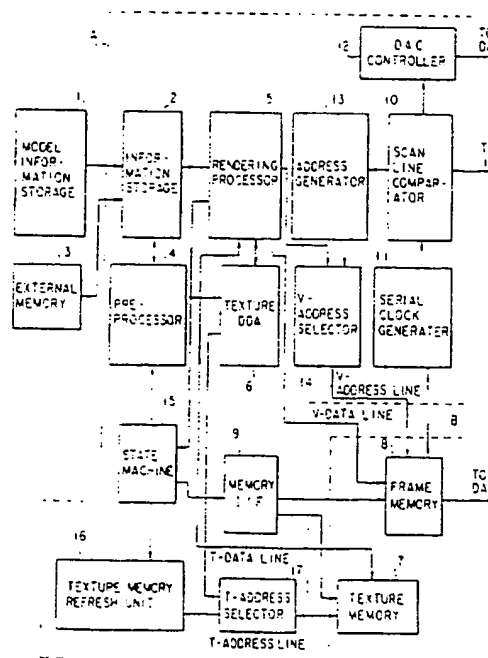
FIG. 2

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EUROPEAN SEARCH REPORT

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	IEEE COMPUTER GRAPHICS AND APPLICATIONS., vol.6, no.10, October 1986, NEW YORK US pages 49 - 55, XP4807 SHIRES 'A NEW VLSI GRAPHICS COPROCESSOR-THE INTEL 82786' * the whole document * ---	1-6	G06F15/72
Y	EP-A-0 438 193 (PHILIPS) * the whole document * ---	1-6	
Y	US-A-4 945 495 (DAIKIN INDUSTRIES) * the whole document * -----	1-6	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			G06T

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	3 October 1994	Burgaud, C